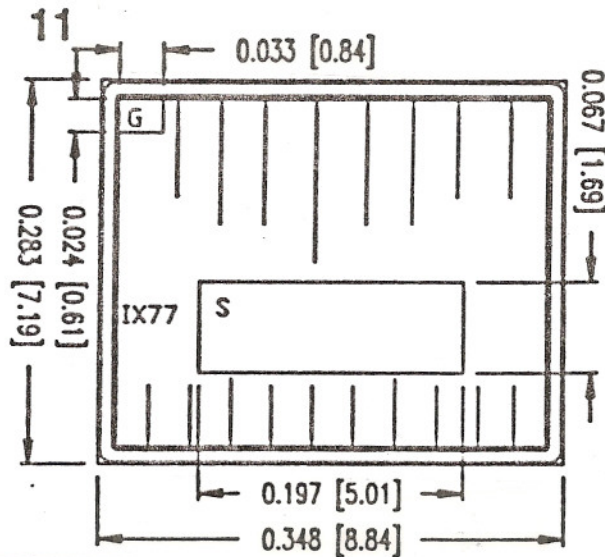




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: Al**  
**Backside: Cr, V/Ni, Au (3 layers)**  
**Backside Potential: Drain**  
**Mask Ref:**  
**Bond Pads (Mils): .004" min**

**APPROVED BY: CB**  
**MFG: IXYS**

**DIE SIZE: .283" x .348"**  
**THICKNESS: .016"**

**DATE: 2/26/01**  
**P/N:IXTD24N50**

DG 10.1.2  
 Rev A 3-4-99